REMARKS

The Office Action dated January 25, 2005, has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. Claims 24-27, 29, 43, 44, 56, 57, 60 and 61 are allowed.

By this Amendment, claim 52 has been canceled as being drawn to a non-elected invention, and claims 53-55, 58 and 59 have been amended. Support for the amendments to these claims can be found on page 8, line 22, to page 9, line 18, of the specification as originally filed. No new matter has been added. Claims 2-8, 10-19, 21, 22, 31-40, 53-55, 58 and 59 are pending and respectfully submitted for consideration.

Claims 2, 3, 7, 10, 11, 14, 16, 18, 21, 22, 31, 32, 35-38, 53-55, 58 and 59 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Higuchi et al. (U.S. Patent No. 6,167,037, "Higuchi") in view of Yanagi (U.S. Patent No. 6,345,045 B1). Higuchi was cited for disclosing many of the claimed elements of the invention with the exception of selecting the correlation value which exceeds the threshold value and storing the selected correlation value in a memory. Yanagi was cited for curing this deficiency. Claims 2, 3 and 7 depend from claim 53; claims 10, 11, 14, 16 and 18 depend from claim 54; claims 21 and 22 depend from claim 55; and claims 31, 32 and 35-38 depend from claim 58.

Claims 13, 33 and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Higuchi in view of Yanagi as applied to claims 10, 11, 31, 32, 54 and 58 above, and further in view of Shibata et al. (U.S. Patent No. 6,115,725, "Shibata"). Higuchi and Yanagi were cited for disclosing many of the claimed elements of the invention with the exception of first and second storage sections provided in a single memory, as recited in claim 13; a register for arbitrarily setting the reference set value, as recited in claim 33;

and a register for arbitrarily setting the path count set value, as recited in claim 39. Shibata was cited for curing these deficiencies.

Claim 17 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Higuchi in view of Yanagi as applied to claims 10, 11 and 54, and further in view of Wilson (U.S. Patent No. 3,680,055). Higuchi and Yanagi were cited for disclosing many of the claimed elements of the invention with the exception of an overflow notification section for notifying a shortage of storage area in at least one of the first and second storage sections when it occurs. Wilson was cited for curing this deficiency.

To the extent that the above-noted rejections remain applicable to the claims currently pending, the Applicants respectfully submit that claims 2, 3, 7, 10, 11, 13, 14, 16-18, 21, 22, 31, 32, 33 35-39, 53-55, 58 and 59 recite subject matter that is neither disclosed nor suggested by the cited references.

Higuchi discloses, in Fig. 9, detecting correlation values by comparing an input signal with a spreading code (S2100), storing all of the detected correlation values in a memory (S2200), selecting the maximum correlation value (S2300), and comparing the maximum correlation value with a threshold value. Unless the maximum correlation value exceeds the threshold value, return to S2100 (S2400 in Fig. 9).

Yanagi discloses a CDMA synchronous capture circuit which calculates correlation values by using a part of received data for the detection of the peak position, and then decides an upper temporal peak position where the correlation values are great. The CDMA synchronous capture circuit calculates the remaining correlation values, giving priority over the temporal peak position, by using the remaining received data, and decides a peak value from the correlation level by adding the above-mentioned two kinds of correlation values.

Shibata discloses references 202 through 205 indicate SRAMs having a memory capacity of 8 kbit that are capable of storing, respectively, 64 code vectors. Each code vector is inputted from the exterior and written in advance in accordance with the predetermined operation. SRAM and memory circuits such as DRAM, EPROM, EEPROM and the like, which are capable of being electrically written at least once, may be employed. Memory circuits into which predetermined code vectors have been written in advance during the pattern formation of semiconductor integrated circuit manufacturing processes, and which cannot be rewritten electrically can be used. The number of vectors which may be stored can be altered in accordance with the design.

Wilson discloses a control lever or bit in a bit position that indicates that an overflow error condition exists and that appropriate corrective action must be taken.

Claim 53 recites a cell search method comprising the steps of detecting correlation values between an input signal and a spreading code; comparing each of the detected correlation values with a threshold value to limit a subject of integration; performing the integration to a correlation value exceeding the threshold value and storing the integration value in a memory, while excluding a correlation value not exceeding the threshold value from the subject of the integration and not storing in a memory; and detecting a correlation peak value in a predetermined unit of slots by the integration values in the memory for a plurality of the slots.

Claim 54 recites a communication synchronization apparatus comprising a detection device that detects correlation values between an input signal and a spreading code generated by the detection device, and detects a correlation peak value in a predetermined unit of slots to detect a synchronization point of the input signal. A comparison section compares each of the detected correlation values with a

predetermined threshold value to limit a subject of integration. A performing section performs the integration to a correlation value exceeding the threshold value and stores the integration value in a memory while excluding a correlation value not exceeding the threshold value from the subject of the integration and not storing in a memory. The detection device detects a correlation peak value in a predetermined unit of slots by the integration values in the memory for a plurality of the slots.

Claim 55 recites a computer-readable storage medium for a communication synchronization apparatus comprising a detection device that detects correlation values between an input signal and a spreading code generated by the detection device and detects a correlation peak value in a predetermined unit of slots to detect a synchronization point of the input signal. The medium stores a program for causing a computer to realize a comparison function of comparing each of the detected correlation values with a predetermined threshold value to limit a subject of integration. A performing section performs the integration to a correlation value exceeding the threshold value and stores the integration value in a memory, while excluding a correlation value not exceeding the threshold value from the subject of the integration and not stored in a memory. The detecting device detects a correlation peak value in a predetermined unit of slots by the integration values in the memory for a plurality of the slots.

Claim 58 recites a communication synchronization apparatus comprising a detection device that detects each slot in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection device. The detection process for correlation value is performed over several slots. The correlation values obtained in the slots are integrated to detect a correlation peak value, and thereby a synchronization point of the input signal is detected. A comparison section compares each

of a calculated integrated correlation value with a reference set value and compares each of the detected correlation values with a predetermined threshold value to limit a subject of integration. A performing section performs the integration to a correlation value exceeding the threshold value and stores the integration value in a memory, while excluding a correlation value not exceeding the threshold value from the subject of the integration and not stored in a memory. The detecting device detects a correlation peak value in a predetermined unit of slots by the integration values in the memory for a plurality of the slots.

Claim 59 recites a communication synchronization apparatus comprising a detection device that detects each slot in a predetermined unit, correlation values between an input signal and a spreading code generated by the detection device. The detection process for correlation value is performed over several slots. The correlation values obtained in the slots are integrated to detect a correlation peak value, and thereby a synchronization point of the input signal is detected. A comparison section compares each of the detected correlation value or each of a value output from a power conversion device for converting the correlation value into a power value, with a reference set value, and compares each of the detected correlation values with a predetermined threshold value to limit a subject of integration. A performing section performs the integration to a correlation value exceeding the threshold value and stores the integration value in a memory, while excluding a correlation value not exceeding the threshold value from the subject of the integration and not stored in a memory. The detecting device detects a correlation peak value in a predetermined unit of slots by the integration values in the memory for a plurality of the slots.

As a result of the claimed invention, a threshold value is provided to limit a subject of integral calculation. A correlation value exceeding the threshold value is integrated and stored in a memory, while a correlation value not exceeding the threshold value is not a subject of integration and is not stored in a memory. With this structure, memory scale is substantially reduced. Furthermore, because a small correlation value, which does not effect a result of the cell search in the future, is not even performed, the integration power consumption of this regard may be reduced. This feature gives a remarkable effect to a mobile terminal of a CDMA system which has problems with shortages of continuous call time and continuous standby time.

Claim 53 recites a cell search method comprising comparing each of the detected correlation values with a threshold value to limit a subject of integration; performing the integration to a correlation value exceeding the threshold value and storing the integration value in a memory, while excluding a correlation value not exceeding the threshold value from the subject of the integration and not storing in a memory. Clams 54, 58 and 59 recite a comparison section for comparing each of the detected correlation values with a predetermined threshold value to limit a subject of integration; and a performing section for performing the integration to a correlation value exceeding the threshold value and storing the integration value in a memory, while excluding a correlation value not exceeding the threshold value from the subject of the integration and not storing in a memory. Claim 55 recites a medium storing a program for causing a computer to realize a comparison function of comparing each of the detected correlation values with a predetermined threshold value to limit a subject of integration; and a performing section for performing the integration to a correlation value exceeding the threshold value and storing the integration value in a memory, while excluding a correlation value not exceeding the threshold value

from the subject of the integration and not storing in a memory.

In contrast, Yanagi discloses, in Fig. 1, that all correlation values detected at a multiplier 141 are integrated by an integrator 142, and then compared with a threshold value at a level detector 26. That is, Yanagi does not disclose the feature of limiting a subject of integration as recited in claims 53-55, 58 and 59.

In Yanagi, all correlation values detected are the subject of integral calculation. To perform a cell search, an integration result of the correlation value needs to be detected in every timing of detecting the correlation value. Therefore, a memory is required to store the currently detected integration result of the integrated correlation value for the integration result of a correlation value at the next and the same timing. In Yanagi, because all correlation values detected are a subject of integration, quite a large-scaled memory is necessary for integral calculation. As such, Yanagi does not disclose or suggest at least the combination of that a cell search is performed by integration values of correlation values for a plurality of slots, that a correlation value exceeding the threshold value to limit a subject of the integration is performed, and that the integration value is stored in a memory, while a correlation value not exceeding the threshold value to limit a subject of the integration is excluded from the subject of the integration and is not stored in a memory, and therefore, fails to cure the deficiencies in Higuchi with respect to claims 53-55, 58 and 59.

Under U.S. patent practice, the PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference

could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002). The Office Action restates the advantages of the present invention to justify the combination of references. There is, however, nothing in the applied references to evidence the desirability of these advantages in the disclosed structure.

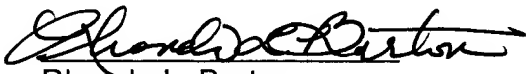
For at least the combination of foregoing reasons, the Applicants respectfully submit that Higuchi, Yanagi, Shibata and Wilson, either singly or in combination, do not support a *prima facie* case of obviousness for purposes of a rejection of claims 53-55, 58 and 59 under 35 U.S.C. § 103.

Claims 2-8 depend from claim 53. Claims 10-19 depend from claim 54. Claims 21 and 22 depend from claim 55. Claims 31-40 depend from claim 58. The Applicants respectfully submit that these dependent claims are allowable at least because of their dependency from allowable base claims 53, 54, 55 and 58. Accordingly, the Applicants respectfully request withdrawal of the rejections, allowance of the claims, and the prompt issuance of a Notice of Allowability.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing Attorney Dkt. No. 108390-00002**.

Respectfully submitted,



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Enclosure: Petition for Extension of Time (two-month)

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